## REMARKS

Claims 1-23 stand rejected under *35 U.S.C. §102(b)* over U. S. Patent No. 6,173,114 to Yanagihara et al. ("Yanagihara") or under *35 U.S.C. §103(a)* over Yanagihara in view of Saito et al. ("Saito"). Claims 3, 5, 8, and 10 stand rejected under *35 U.S.C. §103(a)* as being unpatentable over U. S. Patent No. 6,173,114 to Yanagihara et al. ("Yanagihara") in view of U. S. Patent No. 6,304,173 to Pala et al. ("Pala"). Claims 21 and 23 stand rejected under *35 U.S.C. §103(a)* as being unpatentable over U. S. Patent No. 6,173,114 to Yanagihara et al. ("Yanagihara") in view of U. S. Patent No. 6,523,696 to Saito et al. ("Saito") and in further view of U. S. Patent No. 6,304,173 to Pala et al. ("Pala").

According to *MPEP §2131*, "to anticipate a claim, the reference must teach every element of the claim." A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

According to *MPEP §2143*, "to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)."

The Supreme Court has recently confirmed that under *35 U. S. C. §103*, the scope and content of the prior art are to be determined; differences between the prior art of the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. *KSR International v. Teleflex, Inc.*, 550 U. S. __, at 2

(Sup. Ct. 2007). "Convincing evidence" may be provided for establishing obviousness, *KSR,* at 24.

Regarding independent claims 1, 4, 9, 11, 12, 13, 14, 17, 18, and 22, independent claims 1, 4, 9, 11, 12, 13, 14, 17, 18, and 22 stand rejected under *35 U.S.C. §102(b)* over Yanagihara.

In rejecting claim 1, the Examiner relies on teaching column 2, lines 14-29 and at column 4, lines 20-46. The teaching at column 2, lines 14-29 and at column 4, lines 20-46 of Yanagihara is as follows:

> FIG. 1 shows a structural example of an AV system which incorporates the reproducing device of the present invention. In this example, a DVD player 1 reproduces a video signal from a DVD and supplies that video signal in analog form to an analog television 2. A plurality of (three televisions in this embodiment) digital televisions 3-1 to 3-3 are connected to the DVD player 1 through an AV bus 5. Each digital television 3-1 to 3-3 has a built-in decoder section 4-1 to 4-3, respectively, for decoding the encoded data transmitted from the DVD player 1 via the AV bus 5 and for supplying the decoded data to a respective digital television 3-1 to 3-3 for display.
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> The AV bus 5 may be a digital interface such as IEEE (Institute of Electrical and Electronics Engineers) 1394 High is Performance Serial Bus standard (referred to hereinafter simply as a 1394 protocol). *U. S. Patent No. 6,173,114, column 2 lines 14-29.*
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> The controller 44 executes the processing steps shown in the flow chart of FIG. 6 in accordance with the data quantity of the FIFO 41. In step S11, an inquiry is made as to whether the difference between the write pointer WP, which indicates the writing position of the FIFO 41, and the read pointer RP, which indicates the reading position of the FIFO, is equal to or larger than a first reference value R.sub.L (e.g., an empirically determined value). If the difference between WP and RP is larger than R.sub.L, the FIFO 41 may overflow and the controller 44 outputs a control signal to the drive controller 52 to temporarily stop the access (reproduction operation) of the disc 22 by the pickup 23, as represented by step S12. This prevents the FIFO 41 from overflowing.
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> If in step S11 the difference is determined to be smaller than the reference value R.sub.L, or if the "stop access" processing of step S12 is executed, the routine proceeds to step S13. Here, the controller 44 determines whether the difference between WP and RP is equal to or smaller than a second reference value R.sub.S (which also may be an empirically determined value). If the difference between WP and RP is equal to or smaller than the second reference value R.sub.S, the FIFO 41 may underflow and the routine proceeds to step S14 whereat the controller outputs a control signal to the drive controller 52 to restart the access operation which may have been temporarily stopped in step S12, thereby, preventing the FIFO 41 from underflowing. *U. S. Patent No. 6,173,114, column 4, lines 20-46.*

Claim 1. (Original) A disc playback system comprising a disc drive for reading a coded signal recorded on a disc type recording medium, and transmitting the coded signal through a synchronous channel of a digital bus, and plural display units each receiving the coded signal from the digital bus, and decoding and displaying the coded signal, wherein:

each of the plural display units outputs disc control information including a read command for controlling the disc drive so as to read the coded signal from the disc type recording medium; and

one of the plural display units receives the disc control information from the other display units, and the display unit receives, at least as for the read command, the read commands from all of the other display units which are operating and, thereafter, outputs one read command to the disc drive.

Regarding claim 1, claim 1 recites in combination with numerous additional elements the element "one of the plural display units receives the disc control information from the other display units, and the display unit receives, at least as for the read command, the read commands from all of the other display units which are operating and, thereafter, outputs one read command to the disc drive." Applicants

respectfully assert that applicants cannot locate the highlighted claim element in the specific combination in which it is recited in the relied upon section of Yanagihara. Applicants respectfully assert that the section of Yanagihara relied upon by the Examiner appears to relative wholly to a disc drive unit (it appears that controller 44 in the relied upon section relates to a disc drive unit) and does not relate to a system having display units functioning in the manner as recited in the referenced claim. In order to sustain a *prima facie* case of anticipation, the Examiner must demonstrate that each and every element of the claim is found in the prior art. *MPEP §2131*. If the Examiner wishes to maintain the rejection of claim 1 over *35 U.S.C. §102(b)*, the Examiner is respectfully requested to point out where in Yanagihara there is a teaching relating to the element "one of the plural display units receives the disc control information from the other display units, and the display unit receives, at least as for the read command, the read commands from all of the other display units which are operating and, thereafter, outputs one read command to the disc drive" in the specific combination in which it is recited in claim 1.

In rejecting claim 4, the Examiner relies on teaching at column 2, lines 62-67 and column 3, lines 7-26 of Yanagihara. The teaching at column 2, lines 62-67 and column 3, lines 7-26 of Yanagihara is as follows:

> The output data from the MMU 27 is supplied to a VBR (Variable Bit Rate) control circuit 29 which controls the timing of the data. The time controlled data is supplied to a 1394 transmission circuit 30 which converts the data to the 1394 format, and transmits the converted data to the AV bus 5. *U. S. Patent No. 6,173,114, column 2 lines 62-67.*
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> FIG. 4 shows a structural example of the VBR control circuit 29. The output data from the MMU 27 is supplied to the 1394 transmission circuit 30 via a FIFO (First In First Out) buffer 41. The output data from the MMU 27 is also supplied to a system clock reference (SCR) extraction circuit 42, which extracts the system clock reference (SCR) contained in such data (time information). The extracted SCR is supplied to a comparison circuit 43 and, via switch 45, to a counter 46.
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> The comparison circuit 43 compares the system time clock (STC) (standard time) produced by the counter 46 to the SCR received from the SCR extraction circuit 42, and outputs the comparison result to a controller 44.
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> The controller 44 controls the FIFO 41 in accordance with the comparison result determined by the comparison circuit 43, and also detects the quantity of data in the FIFO 41. The controller 44 supplies a control signal corresponding to the detected data quantity to a drive controller 52 which, in turn, controls the pickup 23 (FIG. 3) in accordance with that control signal. *U. S. Patent No. 6,173,114, column 3 lines 7-26.*
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> Claim 4.(Original) A disc playback system comprising a disc drive for reading a coded signal recorded on a disc type recording medium, and transmitting the coded signal through a synchronous channel of a digital bus, and plural display units each receiving the coded signal from the digital bus, and decoding and displaying the coded signal, wherein:
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> each of the plural display units performs operation on the basis of a periodic signal whose temporal relationship with data on the synchronous channel is constant;
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> one of the plural display units generates decoder control information including at least a playback command, outputs the decoder control information to the other display units, and executes decoder control at a timing when a predetermined time t (t: positive real number) has passed from the n-th periodic signal (n: natural number) after the display unit outputted the decoder control information; and
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> each of the other display units receives the decoder control information, and executes decoder control at a timing when the predetermined time t has passed from the n-th periodic signal after the display unit received the decoder control information.

Regarding claim 4, claim 4 recites in combination with numerous additional elements the element "one of the plural display units...outputs the decoder control information to the other display units, and executes decoder control at a timing when a predetermined time t (t: positive real number) has passed from the n-th periodic signal (n: natural number) after the display unit outputted the decoder control information; and each of the other display units receives the decoder control information, and executes decoder control at a timing when the predetermined time t has passed from the n-th periodic signal after the display unit received the decoder control information." Applicants respectfully assert that applicants cannot locate the highlighted claim element in the specific combination in which it is recited in the relied upon section of Yanagihara. Applicants respectfully assert that the relied upon section of Yanagihara relates to further characteristics of a disc drive unit, and not to a system having display units functioning in the manner as recited in the referenced claim. In order to sustain a *prima facie* case of anticipation, the Examiner must demonstrate that each and every element of the claim is found in the prior art. *MPEP §2131.* If the Examiner wishes to maintain the rejection of claim 4 over *35 U.S.C. §102(b)*, the Examiner is respectfully requested to point out where in Yanagihara there is a teaching relating to element "one of the plural display units...outputs the decoder control information to the other display units, and executes decoder control at a timing when a predetermined time t (t: positive real number) has passed from the n-th periodic signal (n: natural number) after the display unit outputted the decoder control information each of the other display units receives the decoder control information, and executes decoder control at a timing when the predetermined time t has passed from the n-th periodic signal after the display unit received the decoder control information" in the specific combination in which it is recited in claim 4.

In rejecting claim 9, the Examiner relies on teaching at column 3, line 60 to column 4, line 4 of Yanagihara. The teaching at column 3, line 60 to column 4, line 4 of Yanagihara is as follows:

> In the VBR control circuit 29, the SCR extraction circuit 42 extracts the SCR from the data received from the MMU 27. Immediately after starting the reproduction process of the disc 22, initialization processing is performed and the switch 45 is turned on. The SCR extracted by the SCR extraction circuit 42 is loaded into the counter 46 through the switch 45 and the counter

counts the system clock having a frequency of 27 MHz. The counter generates the STC as the reference time and supplies the STC to the comparison circuit 43 which compares the STC received from the counter to the SCR received from the SCR extraction circuit. The comparison result is supplied to the controller 44. *U. S. Patent No. 6,173,114, column 3 line 60 to column 4, line 4.*

Claim 9.(Original) A disc playback system comprising a disc drive for reading a coded signal recorded on a DVD, and transmitting the coded signal through a synchronous channel of a digital bus, and plural display units for receiving the coded signal from the digital bus, and decoding and displaying the coded signal, wherein:
each of the plural display units generates an operation clock of 27MHz from a transmission path clock of the digital bus, and performs decoding operation on the basis of the operation clock.

Regarding claim 9, claim 9 recites in combination with numerous additional elements the element "each of the plural display units generates an operation clock of 27 MHz from a transmission path clock of the digital bus." Applicants respectfully assert that applicants cannot locate the highlighted claim element in the specific combination in which it is recited in the relied upon section of Yanagihara. Applicants respectfully note that the section of Yanagihara referred by the Examiner relates to a clock counted by counter 46, and not a clock that is "generated from a transmission path clock of the digital bus" as is recited in the referenced claim. In order to sustain a *prima facie* case of anticipation, the Examiner must demonstrate that each and every element of the claim is found in the prior art. *MPEP §2131.* If the Examiner wishes to maintain the rejection of claim 9 over *35 U.S.C. §102(b)*, the Examiner is respectfully requested to point out where in Yanagihara there is a teaching relating to the element "each of the plural display units generates an operation clock of 27 MHz from a transmission path clock of the digital bus" in the specific combination in which it is recited in claim 9.

In rejecting claim 11, the Examiner relies on teaching at column 2, lines 14-49 of Yanagihara. The teaching at column 2, lines 14-49 is as follows:

FIG. 1 shows a structural example of an AV system which incorporates the reproducing device of the present invention. In this example, a DVD player 1 reproduces a video signal from a DVD and supplies that video signal in analog form to an analog television 2. A plurality of (three televisions in this embodiment) digital televisions 3-1 to 3-3 are connected to the DVD player 1 through an AV bus 5. Each digital television 3-1 to 3-3 has a built-in decoder section 4-1 to 4-3, respectively, for decoding the encoded data transmitted from the DVD player 1 via the AV bus 5 and for supplying the decoded data to a respective digital television 3-1 to 3-3 for display.

The AV bus 5 may be a digital interface such as IEEE (Institute of Electrical and Electronics Engineers) 1394 High is Performance Serial Bus standard (referred to hereinafter simply as a 1394 protocol).

FIG. 2 shows an example of the internal structure of the DVD player 1. The DVD player 1 includes a driver section 11, a demultiplexer 12 and a decoder section 13. The driver section 11 reproduces data from the disc and outputs the data to the demultiplexer 12 whereat the data is separated into audio data, video data, and sub-picture data. The decoder section 13 includes three built-in decoders for decoding the audio data, video data, and sub-picture data independently. The data decoded by the decoder section 13 is D/A converted by a D/A converter (not shown) and supplied to the analog television 2 (FIG. 1).

The multiplexed output data from the driver section 11 is supplied to the digital televisions, 3-1, 3-2 and 3-3 via the AV bus 5.

FIG. 3 shows a structural example of the driver section 11. A spindle motor 21 drives a disc 22 (recording medium) at a prescribed speed. A pickup 23 irradiates a laser beam onto the disc 22 to reproduce the data recorded therein. An output from the pickup 23 is supplied to a RF circuit 24,... *U. S. Patent No. 6,173,114, column 2 lines 14-49.*

Claim 11.(Original) A display unit for receiving a coded signal which is read from a disc type recording medium by a disc drive, and decoding and displaying the coded signal, including:

a disc control information output means for outputting disc control information including a read command for controlling the disc drive so as to read the coded signal from the disc type recording medium;

wherein the disc control information output means receives disc control information including the read command from other display units connected to the digital bus, and it receives, at least as for the read command, the read commands from all of the other display units connected to the digital bus and, thereafter, outputs one read command to the disc drive.

Regarding claim 11, claim 11 recites in combination with numerous additional elements a display unit having "a disc control information output means...wherein the disc control information output means receives disc control information including the read command from other display units connected to the digital bus, and it receives, at least as for the read command, the read commands from all of the other display units connected to the digital bus and, thereafter, outputs one read command to the disc drive." Applicants respectfully assert that applicants cannot locate the highlighted claim element in the specific combination in which it is recited in the relied upon section of Yanagihara (it appears that controller 44 in the relied upon section relates to a disc drive unit and does not relate to a display unit having the elements as recited in the referenced claim). In order to sustain a *prima facie* case of anticipation, the Examiner must demonstrate that each and every element of the claim is found in the prior art. *MPEP §2131.* If the Examiner wishes to maintain the rejection of claim 11 over *35 U.S.C. §102(b)*, the Examiner is respectfully requested to point out where in Yanagihara there is a teaching relating to a display unit having "a disc control information output means...wherein the disc control information output means receives disc control information including the read command from other display units connected to the digital bus, and it receives, at least as for the read command, the read commands from all of the other display units connected to the digital bus and, thereafter, outputs one read command to the disc drive" in the specific combination in which it is recited in claim 11.

In rejecting claim 12, the Examiner relies on teaching at column 4, lines 5-59, column 5, lines 28-49, column 3, lines 7-26 and column 4, lines 5-59 of Yanagihara. The teaching at column 4, lines 5-59, column 5, lines 28-49, column 3, lines 7-26 and column 4, lines 5-59 of Yanagihara is as follows:

The operation of the controller 44 will be described in conjunction with the flow chart of FIG. 5. In step S1, an inquiry is made as to whether the SCR is equal to the STC. If the SCR extracted from the reproduced data is determined to be equal to the STC, the routine proceeds to step S2 whereat the controller 44 reads a pack having the SCR from the FIFO 41 and permits the FIFO 41 to supply the pack data to the 1394 transmission circuit 30. The 1394 transmission circuit converts the data received from the FIFO 41 to the 1394 format, and supplies the formatted data to each decoder 4-1 to 4-3 of the respective digital televisions 3-1 to 3-3 via the AV bus 5.

The comparison processing of step S1 accounts for the transmission time on the AV Bus 5 by comparing the STC to the SCR minus the transmission time.

The controller 44 executes the processing steps shown in the flow chart of FIG. 6 in accordance with the data quantity of the FIFO 41. In step S11, an inquiry is made as to whether the difference between the write pointer WP, which indicates the writing position of the FIFO 41, and the read pointer RP, which indicates the reading position of the FIFO, is equal to or larger than a first reference value R.sub.L (e.g., an empirically determined value). If the difference between WP and RP is larger than R.sub.L, the FIFO 41 may overflow and the controller 44 outputs a control signal to the drive controller 52 to temporarily stop the access (reproduction operation) of the disc 22 by the pickup 23, as represented by step S12. This prevents the FIFO 41 from overflowing.

If in step S11 the difference is determined to be smaller than the reference value R.sub.L, or if the "stop access" processing of step S12 is executed, the routine proceeds to step S13. Here, the controller 44 determines whether the difference between WP and RP is equal to or smaller than a second reference value R.sub.S (which also may be an empirically determined value). If the difference between WP and RP is equal to or smaller than the second reference value R.sub.S, the FIFO 41 may underflow and the routine proceeds to step S14 whereat the controller outputs a control signal to the drive controller 52 to restart the access operation which may have been temporarily stopped in step S12, thereby, preventing the FIFO 41 from underflowing.

If the difference between WP and RP is determined to be larger than the reference value R.sub.S in step S13, or after completing the restart operation of step S14, the routine returns to step S11, and the steps S11-S14 are repeated.

Since the controller 44 performs the above-noted control operations to prevent the FIFO 41 from overflowing or underflowing, the decoder sections 4-1, 4-2, and 4-3 of the digital televisions 3-1, 3-2 and 3-3, respectively, are also prevented from overflowing or underflowing. Each decoder section 4-1, 4-2 and 4-3 may decode (access) the data immediately after the data is transmitted thereto on the AV bus 5. *U. S. Patent No. 6,173,114, column 4 lines 5-59.*

A receiving circuit 71, operable in accordance with the IEEE 1394 protocol, of the decoder section 4-1 removes the packet header from the data received from the AV bus 5 to return the received data to its original data format. The receiving circuit 71 supplies the reformatted data to a demultiplexer 72 which separates the data into audio data, video data, and sub-picture data. For example, the demultiplexer 72 supplies the video data to a decoder 73 and to a SCR extraction circuit 74. The SCR extraction circuit 74 extracts the SCR from the video data, and supplies the SCR to a PLL circuit 75 which generates a clock signal having a frequency of, for example, 27 MHz which is synchronous with the input SCR and supplies the clock signal to the decoder 73. The decoder 73 decodes the video data in accordance with the clock signal supplied from the PLL circuit 75. The decoded video data is subjected to D/A conversion (not shown) and thereafter supplied to the CRT of the corresponding digital television (e.g. digital TV 3-1).

It is appreciated that although FIG. 7 depicts the system for processing only the video data, the decoder section includes similar systems for decoding the audio data and the sub-picture data. *U. S. Patent No. 6,173,114, column 5 lines 28-49.*

FIG. 4 shows a structural example of the VBR control circuit 29. The output data from the MMU 27 is supplied to the 1394 transmission circuit 30 via a FIFO (First In First Out) buffer 41. The output data from the MMU 27 is also supplied to a system clock reference (SCR) extraction circuit 42, which extracts the system clock reference (SCR) contained in such data (time information). The extracted SCR is supplied to a comparison circuit 43 and, via switch 45, to a counter 46.

The comparison circuit 43 compares the system time clock (STC) (standard time) produced by the counter 46 to the SCR received from the SCR extraction circuit 42, and outputs the comparison result to a controller 44.

The controller 44 controls the FIFO 41 in accordance with the comparison result determined by the comparison circuit 43, and also detects the quantity of data in the FIFO 41. The controller 44 supplies a control signal corresponding to the detected data quantity to a drive controller 52 which, in turn, controls the pickup 23 (FIG. 3) in accordance with that control signal. *U. S. Patent No. 6,173,114, column 3, lines 7-26.*

The operation of the controller 44 will be described in conjunction with the flow chart of FIG. 5. In step S1, an inquiry is made as to whether the SCR is equal to the STC. If the SCR extracted from the reproduced data is determined to be equal to the STC, the routine proceeds to step S2 whereat the controller 44 reads a pack having the SCR from the FIFO 41 and permits the FIFO 41 to supply the pack data to the 1394 transmission circuit 30. The 1394 transmission circuit converts

the data received from the FIFO 41 to the 1394 format, and supplies the formatted data to each decoder 4-1 to 4-3 of the respective digital televisions 3-1 to 3-3 via the AV bus 5.

The comparison processing of step S1 accounts for the transmission time on the AV Bus 5 by comparing the STC to the SCR minus the transmission time.

The controller 44 executes the processing steps shown in the flow chart of FIG. 6 in accordance with the data quantity of the FIFO 41. In step S11, an inquiry is made as to whether the difference between the write pointer WP, which indicates the writing position of the FIFO 41, and the read pointer RP, which indicates the reading position of the FIFO, is equal to or larger than a first reference value R.sub.L (e.g., an empirically determined value). If the difference between WP and RP is larger than R.sub.L, the FIFO 41 may overflow and the controller 44 outputs a control signal to the drive controller 52 to temporarily stop the access (reproduction operation) of the disc 22 by the pickup 23, as represented by step S12. This prevents the FIFO 41 from overflowing.

If in step S11 the difference is determined to be smaller than the reference value R.sub.L, or if the "stop access" processing of step S12 is executed, the routine proceeds to step S13. Here, the controller 44 determines whether the difference between WP and RP is equal to or smaller than a second reference value R.sub.S (which also may be an empirically determined value). If the difference between WP and RP is equal to or smaller than the second reference value R.sub.S, the FIFO 41 may underflow and the routine proceeds to step S14 whereat the controller outputs a control signal to the drive controller 52 to restart the access operation which may have been temporarily stopped in step S12, thereby, preventing the FIFO 41 from underflowing.

If the difference between WP and RP is determined to be larger than the reference value R.sub.S in step S13, or after completing the restart operation of step S14, the routine returns to step S11, and the steps S11-S14 are repeated.

Since the controller 44 performs the above-noted control operations to prevent the FIFO 41 from overflowing or underflowing, the decoder sections 4-1, 4-2, and 4-3 of the digital televisions 3-1, 3-2 and 3-3, respectively, are also prevented from overflowing or underflowing. Each decoder section 4-1, 4-2 and 4-3 may decode (access) the data immediately after the data is transmitted thereto on the AV bus 5. *U. S. Patent No. 6,173,114, column 4 lines 5-59.*

Claim 12. (Original) A display unit for receiving a coded signal which is read from a disc type recording medium by a disc drive and transmitted through a synchronous channel of a digital bus, and decoding and displaying the coded signal,
the display unit performing operation on the basis of a periodic signal whose temporal relationship with data on the synchronous channel is constant; and the display unit comprising:

a decoder control information generation means for generating decoder control information including at least a playback command;

a decoder control information output means for outputting the decoder control information generated by the decoder control information generation means to another display unit connected to the digital bus; and

a decoder control means for executing decoder control, employing the decoder control information generated by the decoder control generation means, at a timing when a predetermined time t (t: positive real number) has passed from the n-th periodic signal (n: natural number) after the decoder control information output means outputted the decoder control information to the other display unit.

Regarding claim 12, claim 12 recites in combination with numerous additional elements a display unit having "a decoder control information output means for outputting the decoder control information generated by the decoder control information generation means to another display unit connected to the digital bus; and a decoder control means for executing decoder control, employing the decoder control information generated by the decoder control generation means, at a timing when a predetermined time t (t: positive real number) has passed from the n-th periodic signal (n: natural number) after the decoder control information output means outputted the decoder control information to the other display unit." Applicants respectfully assert that applicants cannot locate the highlighted claim element in the specific combination in which it is recited in the relied upon section of Yanagihara. Applicants respectfully assert that the relied upon section of Yanagihara relates to further characteristics of a disc drive unit, and not to a display unit functioning in the manner as recited in the referenced claim. In order to sustain

a *prima facie* case of anticipation, the Examiner must demonstrate that each and every element of the claim is found in the prior art. *MPEP §2131*. If the Examiner wishes to maintain the rejection of claim 12 over *35 U.S.C. §102(b)*, the Examiner is respectfully requested to point out where in Yanagihara there is a teaching relating to a display unit having "a decoder control information output means for outputting the decoder control information generated by the decoder control information generation means to another display unit connected to the digital bus; and a decoder control means for executing decoder control, employing the decoder control information generated by the decoder control generation means, at a timing when a predetermined time t (t: positive real number) has passed from the n-th periodic signal (n: natural number) after the decoder control information output means outputted the decoder control information to the other display unit" in the specific combination in which it is recited in claim 12.

In rejecting claim 13, the Examiner relies on teaching at column 4, lines 5-59, column 5, lines 28-49, column 3, lines 7-26 and column 4, lines 5-59 of Yanagihara. The teaching at column 4, lines 5-59, column 5, lines 28-49, column 3, lines 7-26 and column 4, lines 5-59 of Yanagihara is as follows:

> The operation of the controller 44 will be described in conjunction with the flow chart of FIG. 5. In step S1, an inquiry is made as to whether the SCR is equal to the STC. If the SCR extracted from the reproduced data is determined to be equal to the STC, the routine proceeds to step S2 whereat the controller 44 reads a pack having the SCR from the FIFO 41 and permits the FIFO 41 to supply the pack data to the 1394 transmission circuit 30. The 1394 transmission circuit converts the data received from the FIFO 41 to the 1394 format, and supplies the formatted data to each decoder 4-1 to 4-3 of the respective digital televisions 3-1 to 3-3 via the AV bus 5.
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> The comparison processing of step S1 accounts for the transmission time on the AV Bus 5 by comparing the STC to the SCR minus the transmission time.
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> The controller 44 executes the processing steps shown in the flow chart of FIG. 6 in accordance with the data quantity of the FIFO 41. In step S11, an inquiry is made as to whether the difference between the write pointer WP, which indicates the writing position of the FIFO 41, and the read pointer RP, which indicates the reading position of the FIFO, is equal to or larger than a first reference value R.sub.L (e.g., an empirically determined value). If the difference between WP and RP is larger than R.sub.L, the FIFO 41 may overflow and the controller 44 outputs a control signal to the drive controller 52 to temporarily stop the access (reproduction operation) of the disc 22 by the pickup 23, as represented by step S12. This prevents the FIFO 41 from overflowing.
>
> If in step S11 the difference is determined to be smaller than the reference value R.sub.L, or if the "stop access" processing of step S12 is executed, the routine proceeds to step S13. Here, the controller 44 determines whether the difference between WP and RP is equal to or smaller than a second reference value R.sub.S (which also may be an empirically determined value). If the difference between WP and RP is equal to or smaller than the second reference value R.sub.S, the FIFO 41 may underflow and the routine proceeds to step S14 whereat the controller outputs a control signal to the drive controller 52 to restart the access operation which may have been temporarily stopped in step S12, thereby, preventing the FIFO 41 from underflowing.
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> If the difference between WP and RP is determined to be larger than the reference value R.sub.S in step S13, or after completing the restart operation of step S14, the routine returns to step S11, and the steps S11-S14 are repeated.
>
> Since the controller 44 performs the above-noted control operations to prevent the FIFO 41 from overflowing or underflowing, the decoder sections 4-1, 4-2, and 4-3 of the digital televisions 3-

1, 3-2 and 3-3, respectively, are also prevented from overflowing or underflowing. Each decoder section 4-1, 4-2 and 4-3 may decode (access) the data immediately after the data is transmitted thereto on the AV bus 5. *U. S. Patent No. 6,173,114, column 4 lines 5-59.*

A receiving circuit 71, operable in accordance with the IEEE 1394 protocol, of the decoder section 4-1 removes the packet header from the data received from the AV bus 5 to return the received data to its original data format. The receiving circuit 71 supplies the reformatted data to a demultiplexer 72 which separates the data into audio data, video data, and sub-picture data. For example, the demultiplexer 72 supplies the video data to a decoder 73 and to a SCR extraction circuit 74. The SCR extraction circuit 74 extracts the SCR from the video data, and supplies the SCR to a PLL circuit 75 which generates a clock signal having a frequency of, for example, 27 MHz which is synchronous with the input SCR and supplies the clock signal to the decoder 73. The decoder 73 decodes the video data in accordance with the clock signal supplied from the PLL circuit 75. The decoded video data is subjected to D/A conversion (not shown) and thereafter supplied to the CRT of the corresponding digital television (e.g. digital TV 3-1).

It is appreciated that although FIG. 7 depicts the system for processing only the video data, the decoder section includes similar systems for decoding the audio data and the sub-picture data. *U. S. Patent No. 6,173,114, column 5 lines 28-49.*

FIG. 4 shows a structural example of the VBR control circuit 29. The output data from the MMU 27 is supplied to the 1394 transmission circuit 30 via a FIFO (First In First Out) buffer 41. The output data from the MMU 27 is also supplied to a system clock reference (SCR) extraction circuit 42, which extracts the system clock reference (SCR) contained in such data (time information). The extracted SCR is supplied to a comparison circuit 43 and, via switch 45, to a counter 46.

The comparison circuit 43 compares the system time clock (STC) (standard time) produced by the counter 46 to the SCR received from the SCR extraction circuit 42, and outputs the comparison result to a controller 44.

The controller 44 controls the FIFO 41 in accordance with the comparison result determined by the comparison circuit 43, and also detects the quantity of data in the FIFO 41. The controller 44 supplies a control signal corresponding to the detected data quantity to a drive controller 52 which, in turn, controls the pickup 23 (FIG. 3) in accordance with that control signal. *U. S. Patent No. 6,173,114, column 3, lines 7-26.*

The operation of the controller 44 will be described in conjunction with the flow chart of FIG. 5. In step S1, an inquiry is made as to whether the SCR is equal to the STC. If the SCR extracted from the reproduced data is determined to be equal to the STC, the routine proceeds to step S2 whereat the controller 44 reads a pack having the SCR from the FIFO 41 and permits the FIFO 41 to supply the pack data to the 1394 transmission circuit 30. The 1394 transmission circuit converts the data received from the FIFO 41 to the 1394 format, and supplies the formatted data to each decoder 4-1 to 4-3 of the respective digital televisions 3-1 to 3-3 via the AV bus 5.

The comparison processing of step S1 accounts for the transmission time on the AV Bus 5 by comparing the STC to the SCR minus the transmission time.

The controller 44 executes the processing steps shown in the flow chart of FIG. 6 in accordance with the data quantity of the FIFO 41. In step S11, an inquiry is made as to whether the difference between the write pointer WP, which indicates the writing position of the FIFO 41, and the read pointer RP, which indicates the reading position of the FIFO, is equal to or larger than a first reference value R.sub.L (e.g., an empirically determined value). If the difference between WP and RP is larger than R.sub.L, the FIFO 41 may overflow and the controller 44 outputs a control signal to the drive controller 52 to temporarily stop the access (reproduction operation) of the disc 22 by the pickup 23, as represented by step S12. This prevents the FIFO 41 from overflowing.

If in step S11 the difference is determined to be smaller than the reference value R.sub.L, or if the "stop access" processing of step S12 is executed, the routine proceeds to step S13. Here, the controller 44 determines whether the difference between WP and RP is equal to or smaller than a second reference value R.sub.S (which also may be an empirically determined value). If the difference between WP and RP is equal to or smaller than the second reference value R.sub.S, the FIFO 41 may underflow and the routine proceeds to step S14 whereat the controller outputs a control signal to the drive controller 52 to restart the access operation which may have been temporarily stopped in step S12, thereby, preventing the FIFO 41 from underflowing.

If the difference between WP and RP is determined to be larger than the reference value R.sub.S in step S13, or after completing the restart operation of step S14, the routine returns to step S11, and the steps S11-S14 are repeated.

Since the controller 44 performs the above-noted control operations to prevent the FIFO 41 from overflowing or underflowing, the decoder sections 4-1, 4-2, and 4-3 of the digital televisions 3-1, 3-2 and 3-3, respectively, are also prevented from overflowing or underflowing. Each decoder section 4-1, 4-2 and 4-3 may decode (access) the data immediately after the data is transmitted thereto on the AV bus 5. *U. S. Patent No. 6,173,114, column 4 lines 5-59.*

Claim13. (Original) A display unit for receiving a coded signal which is read from a disc type recording medium by a disc drive and transmitted through a synchronous channel of a digital bus, and decoding and displaying the coded signal,
the display unit performing operation on the basis of a periodic signal whose temporal relationship with data on the synchronous channel is constant, and the display unit comprising:

a decoder control information reception means for receiving decoder control information including at least a playback command, from another display unit connected to the digital bus; and
a decoder control means for executing decoder control, employing the decoder control information received by the decoder control reception means, at a timing when a predetermined time t (t: positive real number) has passed from the n-th periodic signal (n: natural number) after the decoder control information reception means received the decoder control information from the other display unit.

Regarding claim 13, claim 13 recites in combination with numerous additional elements a display unit having "a decoder control information reception means for receiving decoder control information including at least a playback command, from another display unit connected to the digital bus; and a decoder control means for executing decoder control, employing the decoder control information received by the decoder control reception means, at a timing when a predetermined time t (t: positive real number) has passed from the n-th periodic signal (n: natural number) after the decoder control information reception means received the decoder control information from the other display unit." Applicants respectfully assert that applicants cannot locate the highlighted claim element in the specific combination in which it is recited in the relied upon section of Yanagihara. Applicants respectfully assert that the relied upon section of Yanagihara relates to further characteristics of a disc drive unit, and not to a display unit functioning in the manner as recited in the referenced claim. In order to sustain a *prima facie* case of anticipation, the Examiner must demonstrate that each and every element of the claim is found in the prior art. *MPEP §2131*. If the Examiner wishes to maintain the rejection of claim 13 over *35 U.S.C. §102(b)*, the Examiner is respectfully requested to point out where in Yanagihara there is a teaching relating to a display unit having "a decoder control information reception means for receiving decoder control information including at least a playback command, from another display unit connected to the digital bus; and wherein the disc control information output means receives disc control information including the read command from other display units connected to the digital bus, and it receives, at least as for the read command, the read commands from all of the other display units connected to the digital bus and, thereafter, outputs one read command to the disc drive" in the specific combination in which it is recited in claim 13.

In rejecting claim 14, the Examiner relies on teaching at column 3, line 60 through column 4, line 4 and column 5, lines 28-49 of Yanagihara. The teaching at

column 3, line 60 through column 4, line 4 and column 5, lines 28-49 of Yanagihara is as follows:

> In the VBR control circuit 29, the SCR extraction circuit 42 extracts the SCR from the data received from the MMU 27. Immediately after starting the reproduction process of the disc 22, initialization processing is performed and the switch 45 is turned on. The SCR extracted by the SCR extraction circuit 42 is loaded into the counter 46 through the switch 45 and the counter counts the system clock having a frequency of 27 MHz. The counter generates the STC as the reference time and supplies the STC to the comparison circuit 43 which compares the STC received from the counter to the SCR received from the SCR extraction circuit. The comparison result is supplied to the controller 44. *U. S. Patent No. 6,173,114, column 3 line 60 to column 4, line 4.*
>
> A receiving circuit 71, operable in accordance with the IEEE 1394 protocol, of the decoder section 4-1 removes the packet header from the data received from the AV bus 5 to return the received data to its original data format. The receiving circuit 71 supplies the reformatted data to a demultiplexer 72 which separates the data into audio data, video data, and sub-picture data. For example, the demultiplexer 72 supplies the video data to a decoder 73 and to a SCR extraction circuit 74. The SCR extraction circuit 74 extracts the SCR from the video data, and supplies the SCR to a PLL circuit 75 which generates a clock signal having a frequency of, for example, 27 MHz which is synchronous with the input SCR and supplies the clock signal to the decoder 73. The decoder 73 decodes the video data in accordance with the clock signal supplied from the PLL circuit 75. The decoded video data is subjected to D/A conversion (not shown) and thereafter supplied to the CRT of the corresponding digital television (e.g. digital TV 3-1).
> It is appreciated that although FIG. 7 depicts the system for processing only the video data, the decoder section includes similar systems for decoding the audio data and the sub-picture data. *U. S. Patent No. 6,173,114, column 5 lines 28-49.*
>
> Claim 14. (Original) A display unit for receiving a coded signal from a digital bus, and decoding and displaying the coded signal, including:
> a decoding clock generation means for generating a decoding clock of 27MHz for performing decoding operation, from a transmission path clock of the digital bus.

Regarding claim 14, claim 14 recites in combination with numerous additional elements the element "a decoding clock generation means for generating a decoding clock of 27 MHz for performing decoding operation, from a transmission path clock of the digital bus." Applicants respectfully assert that applicants cannot locate the highlighted claim element in the specific combination in which it is recited in the relied upon section of Yanagihara. Applicants respectfully note that the section of Yanagihara referred by the Examiner relates to a clock counted by a counter and does not recount to a clock that is "generated from a transmission path clock of the digital bus" as recited in the referenced claim. In order to sustain a *prima facie* case of anticipation, the Examiner must demonstrate that each and every element of the claim is found in the prior art. *MPEP §2131*. If the Examiner wishes to maintain the rejection of claim 14 over *35 U.S.C. §102(b)*, the Examiner is respectfully requested to point out where in Yanagihara there is a teaching relating to the element "a decoding clock generation means for generating a decoding clock of 27 MHz for performing decoding operation, from a transmission path clock of the digital bus" in the specific combination in which it is recited in claim 14.

In rejecting claim 17, the Examiner relies on teaching at column 4, lines 5-59, column 5, lines 28-49, column 3, lines 7-26 and column 4, lines 5-59 of Yanagihara. The teaching at column 4, lines 5-59, column 5, lines 28-49, column 3, lines 7-26 and column 4, lines 5-59 of Yanagihara is as follows:

> The operation of the controller 44 will be described in conjunction with the flow chart of FIG. 5. In step S1, an inquiry is made as to whether the SCR is equal to the STC. If the SCR extracted from the reproduced data is determined to be equal to the STC, the routine proceeds to step S2 whereat the controller 44 reads a pack having the SCR from the FIFO 41 and permits the FIFO 41 to supply the pack data to the 1394 transmission circuit 30. The 1394 transmission circuit converts the data received from the FIFO 41 to the 1394 format, and supplies the formatted data to each decoder 4-1 to 4-3 of the respective digital televisions 3-1 to 3-3 via the AV bus 5.
>
> The comparison processing of step S1 accounts for the transmission time on the AV Bus 5 by comparing the STC to the SCR minus the transmission time.
>
> The controller 44 executes the processing steps shown in the flow chart of FIG. 6 in accordance with the data quantity of the FIFO 41. In step S11, an inquiry is made as to whether the difference between the write pointer WP, which indicates the writing position of the FIFO 41, and the read pointer RP, which indicates the reading position of the FIFO, is equal to or larger than a first reference value R.sub.L (e.g., an empirically determined value). If the difference between WP and RP is larger than R.sub.L, the FIFO 41 may overflow and the controller 44 outputs a control signal to the drive controller 52 to temporarily stop the access (reproduction operation) of the disc 22 by the pickup 23, as represented by step S12. This prevents the FIFO 41 from overflowing.
>
> If in step S11 the difference is determined to be smaller than the reference value R.sub.L, or if the "stop access" processing of step S12 is executed, the routine proceeds to step S13. Here, the controller 44 determines whether the difference between WP and RP is equal to or smaller than a second reference value R.sub.S (which also may be an empirically determined value). If the difference between WP and RP is equal to or smaller than the second reference value R.sub.S, the FIFO 41 may underflow and the routine proceeds to step S14 whereat the controller outputs a control signal to the drive controller 52 to restart the access operation which may have been temporarily stopped in step S12, thereby, preventing the FIFO 41 from underflowing.
>
> If the difference between WP and RP is determined to be larger than the reference value R.sub.S in step S13, or after completing the restart operation of step S14, the routine returns to step S11, and the steps S11-S14 are repeated.
>
> Since the controller 44 performs the above-noted control operations to prevent the FIFO 41 from overflowing or underflowing, the decoder sections 4-1, 4-2, and 4-3 of the digital televisions 3-1, 3-2 and 3-3, respectively, are also prevented from overflowing or underflowing. Each decoder section 4-1, 4-2 and 4-3 may decode (access) the data immediately after the data is transmitted thereto on the AV bus 5. *U. S. Patent No. 6,173,114, column 4 lines 5-59.*

> A receiving circuit 71, operable in accordance with the IEEE 1394 protocol, of the decoder section 4-1 removes the packet header from the data received from the AV bus 5 to return the received data to its original data format. The receiving circuit 71 supplies the reformatted data to a demultiplexer 72 which separates the data into audio data, video data, and sub-picture data. For example, the demultiplexer 72 supplies the video data to a decoder 73 and to a SCR extraction circuit 74. The SCR extraction circuit 74 extracts the SCR from the video data, and supplies the SCR to a PLL circuit 75 which generates a clock signal having a frequency of, for example, 27 MHz which is synchronous with the input SCR and supplies the clock signal to the decoder 73. The decoder 73 decodes the video data in accordance with the clock signal supplied from the PLL circuit 75. The decoded video data is subjected to D/A conversion (not shown) and thereafter supplied to the CRT of the corresponding digital television (e.g. digital TV 3-1).
>
> It is appreciated that although FIG. 7 depicts the system for processing only the video data, the decoder section includes similar systems for decoding the audio data and the sub-picture data. *U. S. Patent No. 6,173,114, column 5 lines 28-49.*

> FIG. 4 shows a structural example of the VBR control circuit 29. The output data from the MMU 27 is supplied to the 1394 transmission circuit 30 via a FIFO (First In First Out) buffer 41. The output data from the MMU 27 is also supplied to a system clock reference (SCR) extraction circuit 42, which extracts the system clock reference (SCR) contained in such data (time information). The extracted SCR is supplied to a comparison circuit 43 and, via switch 45, to a counter 46.
>
> The comparison circuit 43 compares the system time clock (STC) (standard time) produced by the counter 46 to the SCR received from the SCR extraction circuit 42, and outputs the comparison result to a controller 44.
>
> The controller 44 controls the FIFO 41 in accordance with the comparison result determined by the comparison circuit 43, and also detects the quantity of data in the FIFO 41. The controller 44 supplies a control signal corresponding to the detected data quantity to a drive controller 52 which,

in turn, controls the pickup 23 (FIG. 3) in accordance with that control signal. *U. S. Patent No. 6,173,114, column 3, lines 7-26.*

The operation of the controller 44 will be described in conjunction with the flow chart of FIG. 5. In step S1, an inquiry is made as to whether the SCR is equal to the STC. If the SCR extracted from the reproduced data is determined to be equal to the STC, the routine proceeds to step S2 whereat the controller 44 reads a pack having the SCR from the FIFO 41 and permits the FIFO 41 to supply the pack data to the 1394 transmission circuit 30. The 1394 transmission circuit converts the data received from the FIFO 41 to the 1394 format, and supplies the formatted data to each decoder 4-1 to 4-3 of the respective digital televisions 3-1 to 3-3 via the AV bus 5.

The comparison processing of step S1 accounts for the transmission time on the AV Bus 5 by comparing the STC to the SCR minus the transmission time.

The controller 44 executes the processing steps shown in the flow chart of FIG. 6 in accordance with the data quantity of the FIFO 41. In step S11, an inquiry is made as to whether the difference between the write pointer WP, which indicates the writing position of the FIFO 41, and the read pointer RP, which indicates the reading position of the FIFO, is equal to or larger than a first reference value R.sub.L (e.g., an empirically determined value). If the difference between WP and RP is larger than R.sub.L, the FIFO 41 may overflow and the controller 44 outputs a control signal to the drive controller 52 to temporarily stop the access (reproduction operation) of the disc 22 by the pickup 23, as represented by step S12. This prevents the FIFO 41 from overflowing.

If in step S11 the difference is determined to be smaller than the reference value R.sub.L, or if the "stop access" processing of step S12 is executed, the routine proceeds to step S13. Here, the controller 44 determines whether the difference between WP and RP is equal to or smaller than a second reference value R.sub.S (which also may be an empirically determined value). If the difference between WP and RP is equal to or smaller than the second reference value R.sub.S, the FIFO 41 may underflow and the routine proceeds to step S14 whereat the controller outputs a control signal to the drive controller 52 to restart the access operation which may have been temporarily stopped in step S12, thereby, preventing the FIFO 41 from underflowing.

If the difference between WP and RP is determined to be larger than the reference value R.sub.S in step S13, or after completing the restart operation of step S14, the routine returns to step S11, and the steps S11-S14 are repeated.

Since the controller 44 performs the above-noted control operations to prevent the FIFO 41 from overflowing or underflowing, the decoder sections 4-1, 4-2, and 4-3 of the digital televisions 3-1, 3-2 and 3-3, respectively, are also prevented from overflowing or underflowing. Each decoder section 4-1, 4-2 and 4-3 may decode (access) the data immediately after the data is transmitted thereto on the AV bus 5. *U. S. Patent No. 6,173,114, column 4 lines 5-59.*

Claim 17. (Currently Amended) A disc playback system comprising a disc drive for reading and outputting a coded signal recorded on a disc type recording medium, and plural display units for decoding and displaying the coded signal outputted from the disc drive, wherein:

the disc drive is provided with a parameter storage means for holding parameters which are used for display operation ~~of~~ by a display unit performing a display operation and, when another display unit has started up, ~~the disc drive~~ transmits the parameters which are used for display operation by the display unit performing the display operation, to the other display unit which has started up.

Regarding claim 17, claim 17 recites in combination with numerous additional elements a disc playback system comprising a disc drive wherein "the disc drive is provided with a parameter storage means for holding parameters which are used for display operation by a display unit performing a display operation and, when another display unit has started up, transmits the parameters which are used for display operation by the display unit performing the display operation, to the other display unit which has started up." Applicants respectfully assert that applicants cannot locate the highlighted claim element in the specific combination in which it is recited in the relied upon section of Yanagihara. In order to sustain a *prima facie* case of anticipation, the Examiner must demonstrate that each and every element of the claim is found in the prior art. *MPEP §2131.* If the Examiner wishes to maintain the

rejection of claim 17 over *35 U.S.C. §102(b)*, the Examiner is respectfully requested to point out where in Yanagihara there is a teaching relating to a disc playback system comprising a disc drive wherein "the disc drive is provided with a parameter storage means for holding parameters which are used for display operation by a display unit performing a display operation and, when another display unit has started up, transmits the parameters which are used for display operation by the display unit performing the display operation, to the other display unit which has started up." in the specific combination in which it is recited in claim 17.

In rejecting claim 18, the Examiner relies on teaching at column 4, lines 5-59, column 5, lines 28-49, column 3, lines 7-26 and column 4, lines 5-59 of Yanagihara. The teaching at column 4, lines 5-59, column 5, lines 28-49, column 3, lines 7-26 and column 4, lines 5-59 of Yanagihara is as follows:

> The operation of the controller 44 will be described in conjunction with the flow chart of FIG. 5. In step S1, an inquiry is made as to whether the SCR is equal to the STC. If the SCR extracted from the reproduced data is determined to be equal to the STC, the routine proceeds to step S2 whereat the controller 44 reads a pack having the SCR from the FIFO 41 and permits the FIFO 41 to supply the pack data to the 1394 transmission circuit 30. The 1394 transmission circuit converts the data received from the FIFO 41 to the 1394 format, and supplies the formatted data to each decoder 4-1 to 4-3 of the respective digital televisions 3-1 to 3-3 via the AV bus 5.
>
> The comparison processing of step S1 accounts for the transmission time on the AV Bus 5 by comparing the STC to the SCR minus the transmission time.
>
> The controller 44 executes the processing steps shown in the flow chart of FIG. 6 in accordance with the data quantity of the FIFO 41. In step S11, an inquiry is made as to whether the difference between the write pointer WP, which indicates the writing position of the FIFO 41, and the read pointer RP, which indicates the reading position of the FIFO, is equal to or larger than a first reference value R.sub.L (e.g., an empirically determined value). If the difference between WP and RP is larger than R.sub.L, the FIFO 41 may overflow and the controller 44 outputs a control signal to the drive controller 52 to temporarily stop the access (reproduction operation) of the disc 22 by the pickup 23, as represented by step S12. This prevents the FIFO 41 from overflowing.
>
> If in step S11 the difference is determined to be smaller than the reference value R.sub.L, or if the "stop access" processing of step S12 is executed, the routine proceeds to step S13. Here, the controller 44 determines whether the difference between WP and RP is equal to or smaller than a second reference value R.sub.S (which also may be an empirically determined value). If the difference between WP and RP is equal to or smaller than the second reference value R.sub.S, the FIFO 41 may underflow and the routine proceeds to step S14 whereat the controller outputs a control signal to the drive controller 52 to restart the access operation which may have been temporarily stopped in step S12, thereby, preventing the FIFO 41 from underflowing.
>
> If the difference between WP and RP is determined to be larger than the reference value R.sub.S in step S13, or after completing the restart operation of step S14, the routine returns to step S11, and the steps S11-S14 are repeated.
>
> Since the controller 44 performs the above-noted control operations to prevent the FIFO 41 from overflowing or underflowing, the decoder sections 4-1, 4-2, and 4-3 of the digital televisions 3-1, 3-2 and 3-3, respectively, are also prevented from overflowing or underflowing. Each decoder section 4-1, 4-2 and 4-3 may decode (access) the data immediately after the data is transmitted thereto on the AV bus 5. *U. S. Patent No. 6,173,114, column 4 lines 5-59.*
>
> A receiving circuit 71, operable in accordance with the IEEE 1394 protocol, of the decoder section 4-1 removes the packet header from the data received from the AV bus 5 to return the received data to its original data format. The receiving circuit 71 supplies the reformatted data to a demultiplexer 72 which separates the data into audio data, video data, and sub-picture data. For example, the demultiplexer 72 supplies the video data to a decoder 73 and to a SCR extraction circuit 74. The SCR extraction circuit 74 extracts the SCR from the video data, and supplies the SCR to a PLL circuit 75 which generates a clock signal having a frequency of, for example, 27 MHz which is synchronous with the input SCR and supplies the clock signal to the decoder 73. The

decoder 73 decodes the video data in accordance with the clock signal supplied from the PLL circuit 75. The decoded video data is subjected to D/A conversion (not shown) and thereafter supplied to the CRT of the corresponding digital television (e.g. digital TV 3-1).

It is appreciated that although FIG. 7 depicts the system for processing only the video data, the decoder section includes similar systems for decoding the audio data and the sub-picture data. *U. S. Patent No. 6,173,114, column 5 lines 28-49.*

FIG. 4 shows a structural example of the VBR control circuit 29. The output data from the MMU 27 is supplied to the 1394 transmission circuit 30 via a FIFO (First In First Out) buffer 41. The output data from the MMU 27 is also supplied to a system clock reference (SCR) extraction circuit 42, which extracts the system clock reference (SCR) contained in such data (time information). The extracted SCR is supplied to a comparison circuit 43 and, via switch 45, to a counter 46.

The comparison circuit 43 compares the system time clock (STC) (standard time) produced by the counter 46 to the SCR received from the SCR extraction circuit 42, and outputs the comparison result to a controller 44.

The controller 44 controls the FIFO 41 in accordance with the comparison result determined by the comparison circuit 43, and also detects the quantity of data in the FIFO 41. The controller 44 supplies a control signal corresponding to the detected data quantity to a drive controller 52 which, in turn, controls the pickup 23 (FIG. 3) in accordance with that control signal. *U. S. Patent No. 6,173,114, column 3, lines 7-26.*

The operation of the controller 44 will be described in conjunction with the flow chart of FIG. 5. In step S1, an inquiry is made as to whether the SCR is equal to the STC. If the SCR extracted from the reproduced data is determined to be equal to the STC, the routine proceeds to step S2 whereat the controller 44 reads a pack having the SCR from the FIFO 41 and permits the FIFO 41 to supply the pack data to the 1394 transmission circuit 30. The 1394 transmission circuit converts the data received from the FIFO 41 to the 1394 format, and supplies the formatted data to each decoder 4-1 to 4-3 of the respective digital televisions 3-1 to 3-3 via the AV bus 5.

The comparison processing of step S1 accounts for the transmission time on the AV Bus 5 by comparing the STC to the SCR minus the transmission time.

The controller 44 executes the processing steps shown in the flow chart of FIG. 6 in accordance with the data quantity of the FIFO 41. In step S11, an inquiry is made as to whether the difference between the write pointer WP, which indicates the writing position of the FIFO 41, and the read pointer RP, which indicates the reading position of the FIFO, is equal to or larger than a first reference value R.sub.L (e.g., an empirically determined value). If the difference between WP and RP is larger than R.sub.L, the FIFO 41 may overflow and the controller 44 outputs a control signal to the drive controller 52 to temporarily stop the access (reproduction operation) of the disc 22 by the pickup 23, as represented by step S12. This prevents the FIFO 41 from overflowing.

If in step S11 the difference is determined to be smaller than the reference value R.sub.L, or if the "stop access" processing of step S12 is executed, the routine proceeds to step S13. Here, the controller 44 determines whether the difference between WP and RP is equal to or smaller than a second reference value R.sub.S (which also may be an empirically determined value). If the difference between WP and RP is equal to or smaller than the second reference value R.sub.S, the FIFO 41 may underflow and the routine proceeds to step S14 whereat the controller outputs a control signal to the drive controller 52 to restart the access operation which may have been temporarily stopped in step S12, thereby, preventing the FIFO 41 from underflowing.

If the difference between WP and RP is determined to be larger than the reference value R.sub.S in step S13, or after completing the restart operation of step S14, the routine returns to step S11, and the steps S11-S14 are repeated.

Since the controller 44 performs the above-noted control operations to prevent the FIFO 41 from overflowing or underflowing, the decoder sections 4-1, 4-2, and 4-3 of the digital televisions 3-1, 3-2 and 3-3, respectively, are also prevented from overflowing or underflowing. Each decoder section 4-1, 4-2 and 4-3 may decode (access) the data immediately after the data is transmitted thereto on the AV bus 5. *U. S. Patent No. 6,173,114, column 4 lines 5-59.*

Claim 18. (Original) A disc playback system comprising a disc drive for reading and outputting a coded signal recorded on a disc type recording medium, and plural display units for decoding and displaying the coded signal outputted from the disc drive, wherein:

when at least one of the plural display units receives an operation input from a user to the self unit and parameters which are stored in the self unit and used for display operation are altered, the display unit transmits the altered parameters to all of the other display units performing display operations.

Regarding claim 18, claim 18 recites in combination with numerous additional elements the element "when at least one of the plural display units receives an operation input from a user to the self unit and parameters which are stored in the self unit and used for display operation are altered, the display unit transmits the altered parameters to all of the other display units performing display operations."

Applicants respectfully assert that applicants cannot locate the highlighted claim element in the specific combination in which it is recited in the relied upon section of Yanagihara. In order to sustain a *prima facie* case of anticipation, the Examiner must demonstrate that each and every element of the claim is found in the prior art. *MPEP §2131.* If the Examiner wishes to maintain the rejection of claim 18 over *35 U.S.C. §102(b)*, the Examiner is respectfully requested to point out where in Yanagihara there is a teaching relating to the element "when at least one of the plural display units receives an operation input from a user to the self unit and parameters which are stored in the self unit and used for display operation are altered, the display unit transmits the altered parameters to all of the other display units performing display operations" in the specific combination in which it is recited in claim 18.

In rejecting claim 22, the Examiner relies on teaching at column 4, lines 5-59, column 5, lines 28-49, column 3, lines 7-26 and column 4, lines 5-59 of Yanagihara. The teaching at column 4, lines 5-59, column 5, lines 28-49, column 3, lines 7-26 and column 4, lines 5-59 of Yanagihara is as follows:

> The operation of the controller 44 will be described in conjunction with the flow chart of FIG. 5. In step S1, an inquiry is made as to whether the SCR is equal to the STC. If the SCR extracted from the reproduced data is determined to be equal to the STC, the routine proceeds to step S2 whereat the controller 44 reads a pack having the SCR from the FIFO 41 and permits the FIFO 41 to supply the pack data to the 1394 transmission circuit 30. The 1394 transmission circuit converts the data received from the FIFO 41 to the 1394 format, and supplies the formatted data to each decoder 4-1 to 4-3 of the respective digital televisions 3-1 to 3-3 via the AV bus 5.
>
> The comparison processing of step S1 accounts for the transmission time on the AV Bus 5 by comparing the STC to the SCR minus the transmission time.
>
> The controller 44 executes the processing steps shown in the flow chart of FIG. 6 in accordance with the data quantity of the FIFO 41. In step S11, an inquiry is made as to whether the difference between the write pointer WP, which indicates the writing position of the FIFO 41, and the read pointer RP, which indicates the reading position of the FIFO, is equal to or larger than a first reference value R.sub.L (e.g., an empirically determined value). If the difference between WP and RP is larger than R.sub.L, the FIFO 41 may overflow and the controller 44 outputs a control signal to the drive controller 52 to temporarily stop the access (reproduction operation) of the disc 22 by the pickup 23, as represented by step S12. This prevents the FIFO 41 from overflowing.
>
> If in step S11 the difference is determined to be smaller than the reference value R.sub.L, or if the "stop access" processing of step S12 is executed, the routine proceeds to step S13. Here, the controller 44 determines whether the difference between WP and RP is equal to or smaller than a second reference value R.sub.S (which also may be an empirically determined value). If the difference between WP and RP is equal to or smaller than the second reference value R.sub.S, the FIFO 41 may underflow and the routine proceeds to step S14 whereat the controller outputs a control signal to the drive controller 52 to restart the access operation which may have been temporarily stopped in step S12, thereby, preventing the FIFO 41 from underflowing.
>
> If the difference between WP and RP is determined to be larger than the reference value R.sub.S in step S13, or after completing the restart operation of step S14, the routine returns to step S11, and the steps S11-S14 are repeated.
>
> Since the controller 44 performs the above-noted control operations to prevent the FIFO 41 from overflowing or underflowing, the decoder sections 4-1, 4-2, and 4-3 of the digital televisions 3-1, 3-2 and 3-3, respectively, are also prevented from overflowing or underflowing. Each decoder section 4-1, 4-2 and 4-3 may decode (access) the data immediately after the data is transmitted thereto on the AV bus 5. *U. S. Patent No. 6,173,114, column 4 lines 5-59.*

A receiving circuit 71, operable in accordance with the IEEE 1394 protocol, of the decoder section 4-1 removes the packet header from the data received from the AV bus 5 to return the received data to its original data format. The receiving circuit 71 supplies the reformatted data to a demultiplexer 72 which separates the data into audio data, video data, and sub-picture data. For example, the demultiplexer 72 supplies the video data to a decoder 73 and to a SCR extraction circuit 74. The SCR extraction circuit 74 extracts the SCR from the video data, and supplies the SCR to a PLL circuit 75 which generates a clock signal having a frequency of, for example, 27 MHz which is synchronous with the input SCR and supplies the clock signal to the decoder 73. The decoder 73 decodes the video data in accordance with the clock signal supplied from the PLL circuit 75. The decoded video data is subjected to D/A conversion (not shown) and thereafter supplied to the CRT of the corresponding digital television (e.g. digital TV 3-1).

It is appreciated that although FIG. 7 depicts the system for processing only the video data, the decoder section includes similar systems for decoding the audio data and the sub-picture data. *U. S. Patent No. 6,173,114, column 5 lines 28-49.*

FIG. 4 shows a structural example of the VBR control circuit 29. The output data from the MMU 27 is supplied to the 1394 transmission circuit 30 via a FIFO (First In First Out) buffer 41. The output data from the MMU 27 is also supplied to a system clock reference (SCR) extraction circuit 42, which extracts the system clock reference (SCR) contained in such data (time information). The extracted SCR is supplied to a comparison circuit 43 and, via switch 45, to a counter 46.

The comparison circuit 43 compares the system time clock (STC) (standard time) produced by the counter 46 to the SCR received from the SCR extraction circuit 42, and outputs the comparison result to a controller 44.

The controller 44 controls the FIFO 41 in accordance with the comparison result determined by the comparison circuit 43, and also detects the quantity of data in the FIFO 41. The controller 44 supplies a control signal corresponding to the detected data quantity to a drive controller 52 which, in turn, controls the pickup 23 (FIG. 3) in accordance with that control signal. *U. S. Patent No. 6,173,114, column 3, lines 7-26.*

The operation of the controller 44 will be described in conjunction with the flow chart of FIG. 5. In step S1, an inquiry is made as to whether the SCR is equal to the STC. If the SCR extracted from the reproduced data is determined to be equal to the STC, the routine proceeds to step S2 whereat the controller 44 reads a pack having the SCR from the FIFO 41 and permits the FIFO 41 to supply the pack data to the 1394 transmission circuit 30. The 1394 transmission circuit converts the data received from the FIFO 41 to the 1394 format, and supplies the formatted data to each decoder 4-1 to 4-3 of the respective digital televisions 3-1 to 3-3 via the AV bus 5.

The comparison processing of step S1 accounts for the transmission time on the AV Bus 5 by comparing the STC to the SCR minus the transmission time.

The controller 44 executes the processing steps shown in the flow chart of FIG. 6 in accordance with the data quantity of the FIFO 41. In step S11, an inquiry is made as to whether the difference between the write pointer WP, which indicates the writing position of the FIFO 41, and the read pointer RP, which indicates the reading position of the FIFO, is equal to or larger than a first reference value R.sub.L (e.g., an empirically determined value). If the difference between WP and RP is larger than R.sub.L, the FIFO 41 may overflow and the controller 44 outputs a control signal to the drive controller 52 to temporarily stop the access (reproduction operation) of the disc 22 by the pickup 23, as represented by step S12. This prevents the FIFO 41 from overflowing.

If in step S11 the difference is determined to be smaller than the reference value R.sub.L, or if the "stop access" processing of step S12 is executed, the routine proceeds to step S13. Here, the controller 44 determines whether the difference between WP and RP is equal to or smaller than a second reference value R.sub.S (which also may be an empirically determined value). If the difference between WP and RP is equal to or smaller than the second reference value R.sub.S, the FIFO 41 may underflow and the routine proceeds to step S14 whereat the controller outputs a control signal to the drive controller 52 to restart the access operation which may have been temporarily stopped in step S12, thereby, preventing the FIFO 41 from underflowing.

If the difference between WP and RP is determined to be larger than the reference value R.sub.S in step S13, or after completing the restart operation of step S14, the routine returns to step S11, and the steps S11-S14 are repeated.

Since the controller 44 performs the above-noted control operations to prevent the FIFO 41 from overflowing or underflowing, the decoder sections 4-1, 4-2, and 4-3 of the digital televisions 3-1, 3-2 and 3-3, respectively, are also prevented from overflowing or underflowing. Each decoder section 4-1, 4-2 and 4-3 may decode (access) the data immediately after the data is transmitted thereto on the AV bus 5. *U. S. Patent No. 6,173,114, column 4 lines 5-59.*

Claim 22. (Original) A disc playback system comprising a disc drive for reading and outputting a coded signal recorded on a disc type recording medium, and plural display units for decoding and displaying the coded signal outputted from the disc drive, wherein:
the display units include decoding means for decoding the coded signal; and
one of the display units transmits a control signal to the decoding means of the other display units.

Regarding claim 22, claim 22 recites in combination with numerous additional elements the element "the display units include decoding means for decoding the

coded signal; and one of the display units transmits a control signal to the decoding means of the other display units." Applicants respectfully assert that applicants cannot locate the highlighted claim element in the specific combination in which it is recited in the relied upon section of Yanagihara. In order to sustain a *prima facie* case of anticipation, the Examiner must demonstrate that each and every element of the claim is found in the prior art. *MPEP §2131.* If the Examiner wishes to maintain the rejection of claim 22 over *35 U.S.C. §102(b)*, the Examiner is respectfully requested to point out where in Yanagihara there is a teaching relating to the element "the display units include decoding means for decoding the coded signal; and one of the display units transmits a control signal to the decoding means of the other display units" in the specific combination in which it is recited in claim 22.

Further regarding claims 12, 13, 17, 18, and 22, the rejection of claims 12, 13, 17, 18, and 22 is further traversed as being in improper omnibus form. This rejection is believed to be improper as an "improperly expressed rejection" in the form of an omnibus rejection as prohibited. According to the *MPEP §707.07(d),* Improperly Expressed Rejections, an omnibus rejection of the claim "on the references and for the reasons of record" should be avoided and a plurality of claims should never be grouped together in a common rejection, unless that rejection is equally applicable to all claims in the group.

If the Examiner wishes to maintain the rejection of claims 12, 13, 17, 18, and 22 in its proper form, the Examiner is respectfully requested to explain how the rejection of claims 12, 13, 17, 18, and 22 is application to each claim of the purported group 12, 13, 17, 18, and 22.

Regarding claims 15, 16, 19, and 20, claims 15, 16, 19, and 20 stand rejected under *35 U.S.C. §103* as being obvious over Yanagihara in view of Saito.

Regarding claim 15, claim 15 recites in combination with numerous additional elements the element of "a parameter control means performing a control such that a display unit which is performing display operation holds parameters used for the display operation and, when another display unit has started up, the display unit performing display operation transmits the parameters to the other display unit which

has started up." In rejecting claim 15 the Examiner has asserted generally that Saito discloses a system that "allows for parameters for various systems." However, applicants respectfully assert that applicants cannot find an assertion by the Examiner that the combination of Yanagihara and Saito includes "a parameter control means performing a control such that a display unit which is performing display operation holds parameters used for the display operation and, when another display unit has started up, the display unit performing display operation transmits the parameters to the other display unit which has started up" in the specific combination in which the highlighted elements are recited in claim 15. In order to establish a *prima facie* case of obviousness, the Examiner must establish that the relied upon art has each and every claim element. *MPEP §2143. See also KSR International v. Teleflex, Inc.*, 550 U. S. __, at 2 (Sup. Ct. 2007) (differences between prior art and claims at issue are resolved in determining obviousness). If the Examiner wishes to maintain the rejection of claim 15, the Examiner is respectfully requested to identify where in the combination of Yanagihara and Saito there is a teaching or suggestion relating to "a parameter control means performing a control such that a display unit which is performing display operation holds parameters used for the display operation and, when another display unit has started up, the display unit performing display operation transmits the parameters to the other display unit which has started up" in the specific combination in which the highlighted elements are recited in claim 15.

Regarding claim 16, claim 16 recited in combination with numerous additional elements the element of "one of the display units performing display operations transmits parameters which are stored in the self unit and used for the display operation, to another display unit which has started up." Applicants respectfully note that in rejecting claim 16, the Examiner has not referenced the highlighted elements of claim 16; but rather, has referenced elements recited in claim 16. If the Examiner wishes to maintain the rejection of claim 16 over Yanagihara and Saito, the Examiner is respectfully requested to identify where in the relied upon prior art there is a teaching related to the element of "one of the display units performing display operations transmits parameters which are stored in the self unit and used for the

display operation, to another display unit which has started up" in the specific combination in which the highlighted elements are recited in claim 16.

Regarding claim 19, claim 19 recites in combination with numerous additional elements the element of "one of the display units performing display operations transmits parameters which are stored in the self unit and used for the display operation, to another display unit which has started up." Applicants respectfully note that in rejecting claim 19, the Examiner has not referenced the highlighted elements of claim 19; but rather, has referenced elements recited in claim 19. If the Examiner wishes to maintain the rejection of claim 19 over Yanagihara and Saito, the Examiner is respectfully requested to identify where in the relied upon prior art there is a teaching related to the element of "one of the display units performing display operations transmits parameters which are stored in the self unit and used for the display operation, to another display unit which has started up" in the specific combination in which the highlighted elements are recited in claim 19.

Further regarding the rejection of claims 15, 16, 19, and 20, the rejection of claims 15, 16, 19, and 20 is traversed for the Examiner having failed to establish that there is a motivation to combine Yanagihara and Saito. It is noted that in attempting to establish motivation, the Examiner has merely recited a function of an element of the secondary reference ("Saito et al. teaches Yanagihara et al. to use of storing parameters for various systems to allow for interchanging of systems while still keeping user parameters"). While establishing motivation necessarily involves an inquiry into the teachings of the primary reference, the Examiner has presented a rationale for there being motivation without considering the teachings of the primary reference. Accordingly, applicants respectfully assert that the Examiner has failed to establish that there is motivation to combine Yanagihara with Saito.

Further regarding the rejection of claims 15, 16, 19, and 20, the rejection is traversed in that the Examiner has failed to specify a section of the primary reference relied upon. While the Examiner generally asserts that the primary reference has certain elements of the claims, the Examiner fails to specify any specific passage of the primary reference. In rejecting claims for want of novelty or for obviousness, the

Examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified. *37 C.F.R. §1.104.*

Further regarding the rejection of claims 15, 16, 19, and 20, the rejection is traversed as being in the form of an improper omnibus rejection. According to the *MPEP §707.07(d),* Improperly Expressed Rejections, an omnibus rejection of the claim "on the references and for the reasons of record" should be avoided and a plurality of claims should never be grouped together in a common rejection, unless that rejection is equally applicable to all claims in the group.

Regarding the claims discussed herein, the applicants' selective treatment and emphasis of independent claims of the application should not be taken as an indication that the applicants believe that the Examiner's dependent claim rejections are otherwise sufficient. In fact, it is noted in the January 12, 2007 Office action, that the dependent claims are rejected without substantial, and in certain instances, without any reference to the limitations of the dependent claims in combination with the base claim elements. Applicants expressly reserve the right to present arguments traversing the propriety of the dependent claim rejections later in the prosecution of this or another application.

While the applicants herein may have highlighted a particular claim element of a claim for purposes of demonstrating an insufficiency of an examination on the part of an Examiner, the applicants highlighting of a particular claim element for such limited purpose should not be taken to indicate that the applicants have taken the position that a particular claim element constitutes the sole basis for patentability out of the context of additional combinations of elements of the claim or claims in which it is present.

Accordingly, in view of the above amendments and remarks, applicants believe all of the claims of the present application to be in condition for.

If the Examiner believes that contact with applicants' attorney would be advantageous toward the disposition of this case, the Examiner is herein requested to call applicants' representative at the phone number listed below.

The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to deposit Account No. 50-0289.

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Respectfully submitted,

By _____

George S. Blasiak
Registration No.: 37,283
MARJAMA & BILINSKI LLP
250 South Clinton Street
Suite 300
Syracuse, New York 13202
(315) 425-9000
Customer No. 20874

GSB/bs